REMARKS

Applicants have carefully considered the April 14, 2005 Office Action, and the amendments above together with the comments that follow are presented in a bona fide effort to address all issues raised in that Action and thereby place this case in condition for allowance. Claims 1-13 are pending in this application. In response to the Office Action dated April 14, 2005, claims 1-13 have been amended and the specification at page 12 has been amended. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment should be apparent throughout the originally filed disclosure as, for example, the depicted embodiments and related discussion thereof in the written description of the specification.

At page 2 of the Office action, the Examiner rejected claims 1 and 11 for lack of enabling support, under the first paragraph of 35 U.S.C. § 112. The Examiner asserted that two phrases in these claims do not read on or are contrary to the embodiments disclosed in the specification. Applicants respectfully request reconsideration and withdrawal of the rejection in view of the foregoing amendments to claims 1 and 11 and the following remarks.

Independent claims 1 and 11 have been amended, in pertinent part, to describe a second comparator which detects a gate voltage of the power semiconductor device to output a second detection signal, when the detected gate signal exceeds a second reference voltage which is set to be lower than a line power voltage of a drive circuit for outputting a drive signal that drives the power semiconductor device and higher than a terraced voltage of the power semiconductor device. As described on page 10, lines 1-19 of the written description of the specification, the second reference voltage (V2) is set at a certain value in a predetermined range. In other words,

the second reference voltage (9 volts) is higher than the terraced voltage (7 volts) and lower than the power supply voltage (15 volts). The predetermined second reference voltage (V2) is supplied to one input terminal of the second comparator (COMP2). Applicants respectfully submit that in view of the foregoing amendments to claims 1 and 11, the specification fully supports the present claims in such a way as to enable one skilled in the art to make and/or use the invention.

With respect to the Examiner's first paragraph rejection under 35 U.S.C. § 112, on page 3 of the Office action, Applicants submit that contrary to the Examiner's assertion, claims 1 and 11 properly define the operation of the protection circuit. The disclosed AND logic circuit issues logic "1" when both of the inputs are "1", and otherwise issues logic "0". That is, the logic means outputs a protection start signal when both of the first and second detection signals are outputted. The Examiner's attention is directed to the enclosed copy of a product specification "DATA SHEET" of Philips AND gates in which the AND logic output logic "H" when both of the inputs are logic "H". Applicants, therefore, respectfully submit that the specification fully supports the present claims in such a way as to enable one skilled in the art to make and/or use the invention.

Independent claims 1 and 11 have also been amended to replace the phrase "power management semiconductor device" with "power semiconductor device". Support for the amendment is found in the written description of the specification at page 7, line 10. Moreover, independent claims 1 and 11 now recite that the power semiconductor device is a trench type power semiconductor device based on the description in page 9, line 18 of the specification. Independent claim 11 has been amended to describe an inverter for converting DC current to AC

current, which is supported in the depicted embodiments (FIG. 5) and related discussion thereof in the written description of the specification (page 14, line 20 to page 15, line 6).

The Examiner objected to the specification for substantially the same reasons set forth in the rejection under the first paragraph of 35 U.S.C. § 112. Further, the Examiner objected to the drawings for alleged failure to show the elements of original claims 1 and 11 that were allegedly not supported by the disclosure. In view of the foregoing amendments and remarks regarding the rejection under the first paragraph of 35 U.S.C. § 112, Applicants respectfully submit that the objections to the specification and drawings are rendered moot.

Claims 5-8 were rejected under 35 U.S.C. § 112, second paragraph. Applicants respectfully traverse the rejection in view of the foregoing amendments to claims 5-8. The allegedly indefinite phrase "electrically continuous" has been removed form the claims. Moreover, claims 5-8 have been amended to describe that the first reference voltage of the comparator is set at a voltage which is higher than an On-state collector voltage and lower than a line power voltage of the drive circuit. As described at page 9, lines 21-28 of the specification, the first reference voltage (V1) is set at a certain value in a predetermined range. Accordingly, one having ordinary skill in the art would not have difficulty understanding the scope of the presently claimed invention, particularly when reasonably interpreted in light of the supporting specification. Therefore, it is respectfully submitted that the imposed rejection of claims 5-8 under 35 U.S.C. § 112, second paragraph is not legally viable and hence, Applicants solicit withdrawal thereof.

Applicants note that dependent claim 2 has been amended to describe that the gate voltage is divided by the resistances (see R1 and R2 in Fig. 3) and the divided voltage is supplied to one input terminal (-) of the second comparator. The specification has been amended in

conformity with the amendment to claim 2, wherein the term "separated" at page 12, lines 20 and 21 of the specification has been changed to "divided" (both occurrences).

Claims 1-4 were rejected under 35 U.S.C. § 102(b) as anticipated by Kimura et al. (U.S. Patent No. 5,210,479, hereinafter "Kimura"). Applicants respectfully traverse.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. Moreover, in imposing the rejection under 35 U.S.C. § 102, the Examiner is required to specifically identify wherein an applied reference is perceived to identically disclose each feature of a claim. That burden has not been discharged. Moreover, there are significant differences between the claimed invention (claim 1) and the device disclosed by Kimura that would preclude the factual determination that Kimura identically describes the subject matter of claim 1 within the meaning of 35 U.S.C. § 102.

As Applicants have described in the specification, at page 9, lines 12-20, the collector voltage and the gate voltage of a trench type power semiconductor device are compared with the respective reference voltages by the separate comparators, and when the both of the collector voltage and the gate voltage exceed the respective reference voltages, the protection start signal is generated to reduce the gate voltage so as to protect the trench type power semiconductor device, which has lower gate terraced voltage.

Claim 1 describes, in pertinent part, that when the collector voltage and the gate voltage exceed the first reference voltage and the second reference voltage, respectively, the protection signal is produced. Kimura fails to identically disclose or remotely suggest producing a protection signal when the collector voltage and the gate voltage exceed the first and second

reference voltages, respectively. Therefore, it is respectfully submitted that the imposed rejection of claims 1-4 under 35 U.S.C. § 102 is not legally viable and hence, Applicants solicit withdrawal thereof.

Dependent claims 5-8 were rejected under 35 U.S.C. § 103 as unpatentable over Kimura in combination with an excerpt from a textbook by Horowitz et al. Dependent claims 9-10 were rejected under 35 U.S.C. § 103 as unpatentable over Kimura alone. Applicants submit that claims 9-10 are free from the applied art in view of their dependency from independent claim 1. With respect to claims 5-8, the secondary reference (Horowitz et al.) does not cure the argued deficiencies of Kimura. Thus, even if the applied references are combined as suggested by the Examiner, and Applicants do not agree that the requisite realistic motivation has been established, the subject matter of claims 5-8 will not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). Therefore, it is respectfully submitted that the imposed rejections of claims 5-10 under 35 U.S.C. § 103 are not legally viable and should be withdrawn.

Claims 11-13 were rejected under 35 U.S.C. § 103 as unpatentable over Wackner et al. (U.S. Patent No. 6,812,586, hereinafter "Wackner") in view of Kimura. Applicants respectfully traverse the rejection.

Independent claim 11, as with independent claim 1, describes that when the collector voltage and the gate voltage exceed the first reference voltage and the second reference voltage, respectively, the protection signal is produced. Neither Wackner nor Kimura discloses or remotely suggests producing a protection signal when the collector voltage and the gate voltage exceed the first and second reference voltages, respectively. Therefore, it is respectfully

submitted that the imposed rejection of claims 11-13 under 35 U.S.C. § 103 is not legally viable and hence, solicit withdrawal thereof.

Based upon the arguments submitted *supra*, it should be apparent that a prima facie basis to deny patentability to the claimed invention has not been established for want of the requisite factual basis and lack of the requisite realistic motivation. Moreover, there are potent indicia of nonobviousness of record which undermine the Examiner's obviousness conclusion. Applicants submit that none of the applied references cited by the Examiner, teaches the problem addressed and solved by the present claimed subject matter, as described one page 2, line 23 through page 3, line 3 of the present specification. Indeed, Applicants respectfully submit that the problem addressed and solved by the claimed inventions is a potent indicium of nonobviousness. *Jones v. Hardy* , 727 F.2d 1524, 220 USPQ 1021 (Fed. Cir. 1984). Upon giving due consideration to the nonobviousness indicia of record, stemming from the problem addressed and solved by the present invention and the evidence in the specification, the conclusion appears inescapable that one having ordinary skill in the art would not have found the claimed invention as a whole obvious within the meaning of 35 U.S.C. § 103. *In re Piasecki*, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

It is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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FUNCTION TABLE

See note 1.

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC1G08GW	−40 to +125 °C	5	SC-88A	plastic	SOT353	AE
74AHCT1G08GW	−40 to +125 °C	5	SC-88A	plastic	SOT353	CE
74AHC1G08GV	−40 to +125 °C	5	SC-74A	plastic	SOT753	A08
74AHCT1G08GV	−40 to +125 °C	5	SC-74A	plastic	SOT753	C08

PINNING

PIN	SYMBOL	DESCRIPTION
1	B	data input B
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

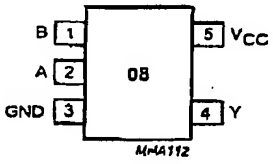

Fig.1 Pin configuration.

Fig.2 Logic symbol.